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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,096	03/01/2004	Errol Todd Ryan	H1840	2466

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THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/791,096	RYAN ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/01/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the tungsten nitride contact liners" on page 11, line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 11, 12, 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929).

Regarding claims 1 and 11, Chang teaches an integrated circuit and a method of forming the integrated circuit comprising providing a semiconductor substrate (**200** in Fig. 2D); forming a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and forming a nickel silicide on the

source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10). Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming contact liners in the contact holes (tungsten nitride, paragraph 0021); and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 2, Chang and Lim together teach the method of claim 1. Lim further teaches that forming the tungsten nitride contact liners uses an atomic layer deposition process (paragraph 0021).

Regarding claim 3, Chang and Lim together teach the method of claim 1. Lim further teaches forming the contact liners at a temperature of less than or equal to about the thermal budget for the silicide, indicated in the instant specification on page 10, lines 23-24 to be 400 – 450 °C (paragraph 0021).

Regarding claims 4 and 12, Chang and Lim together teach the method of claims 1 and 11. Chang further teaches that forming the silicide forms a nickel silicide (column 4, line 56 – column 5, line 10).

Regarding claims 5 and 15-16, Chang and Lim together teach the method of claim 1 and 11. Lim further teaches that forming the contacts forms a tungsten material (paragraph 0026); and forming the contact liners forms a tungsten nitride material (paragraph 0021).

Regarding claims 6 and 17, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (**200** in Fig. 2D); forming a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10). Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes (paragraph 0021); and forming tungsten contacts in the contact holes over the contact liners (paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 7, Chang and Lim together teach the method of claim 6. Lim further teaches that forming the tungsten nitride liners uses an atomic layer deposition process (paragraph 0021).

Regarding claim 8, Chang and Lim together teach the method of claim 6. Lim further teaches forming the tungsten nitride contact liners at a temperature of less than or equal to about 400 degrees centigrade (paragraph 0021).

Regarding claim 20, Chang and Lim together teach the method of claim 17. Chang further teaches that the gate and source and drain regions are ion-implanted with arsenic prior to the formation of nickel silicide on the gate and source and drain regions, so the nickel silicide further comprises arsenic doping (column 4, lines 23-39).

Claims 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claims 6, 11, and 17 above, and further in view of Tseng (U.S. 2005/0035460).

Regarding claims 9, 13, and 18, Chang and Lim together teach the method of claim 6 and the device of claims 11 and 17 (note 35 U.S.C. 103(a) rejections above). They do not teach that forming the nickel silicide uses an ultra-thin thickness of a nickel silicide.

Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Claims 10, 14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claims 6, 11, and 17 above, and further in view of Tseng (U.S. 2005/0035460) and Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claims 10, 14, and 19, Chang and Lim together teach the method of claim 6 and the device of claims 11 and 17 (note 35 U.S.C. 103(a) rejections above). They do not teach that the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Tseng teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Levy et al. (U.S. 2004/0142557) teaches ALD methods for depositing tungsten nitride in contact holes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER